Docket: 8021-160 (SS-18118-US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Sun, et al. Examiner: Thanh V. Pham

Serial No.: 10/621,292 Group Art Unit: 2894

Filed: July 17, 2003
For: **METHOD OF FABRICATING SEMICONDUCTOR DEVICE USING A NICKEL SALICIDE PROCESS**

Mail Stop Appeal Brief--Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO EXAMINER'S ANSWER STATING NEW GROUNDS OF REJECTION

Sir:

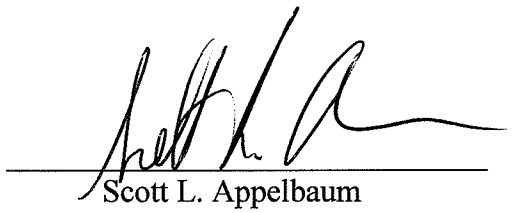
In response to the Examiner's Answers dated May 27, 2009 and April 13, 2009 stating the Examiner's new grounds of rejection, Applicants hereby request that the Appeal filed on July 19, 2007 in connection with the above-referenced patent-application be maintained. The only new ground of rejection presented in the above-mentioned Examiner's answers is that dependent claims 29-30 have now been regrouped to be rejected along with their respective independent claims 19 and 23 under Doan in view of Takeuchi and Maex and further in view of Catabay, Jaiswal and Hill. The above is the only new ground of rejection presented in this case, with the remainder of the claims rejected as detailed in the Final Office Action dated April 3, 2007

In this regard, Applicants are submitting herewith a Reply brief in response to the above-mentioned Examiner's answers dated May 27, 2009 and April 13, 2009 which

addresses the above-mentioned new grounds of rejection as set forth in 37 C.F.R. 41.37 (c) (1) (vii) and is in compliance with the other requirements of 37 C.F.R. 41.37 (c).

Respectfully submitted,

Dated: June 12, 2009



Scott L. Appelbaum
Reg. No. 41,587
Attorney for Applicants

F. CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, NY 11797
(516) 692-8888

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REPLY BRIEF TO EXAMINER'S ANSWER

Sir:

In response to the Examiner's Answers dated May 27, 2009 and April 13, 2009 stating the Examiner's new grounds of rejection in connection with the above-referenced patent application, please consider the following,

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1. REAL PARTY IN INTEREST

The real party in interest is Samsung Electronics Co., Ltd, by virtue of assignment dated June 30, 2003 and recorded July 17, 2003 in the United States Patent and Trademark Office at reel 014309 and frame 0465 for the subject application.

2. RELATED APPEALS AND INTERFERENCES

None.

3. STATUS OF THE CLAIMS

Claims 1, 2, 5-8, 12 13, 16-19, 22, 23, and 26-31 are pending and stand rejected. Claims 1, 2, 5-8, 12 13, 16-19, 22, 23, and 26-31 are under appeal. Claims 3, 4, 9-11, 14, 15, 20, 21, 24 and 25 have been canceled. A copy of the claims under appeal is presented in the Claims Appendix attached herewith.

4. STATUS OF THE AMENDMENTS

No amendments were filed in response to the Final Office Action in this case.

5. SUMMARY OF CLAIMED SUBJECT MATTER

It is to be understood that the following description of the claimed subject matter and references to the specification and drawings are for illustrative purposes only to provide some context for the claimed subject matter, but shall not be construed as placing any limitations thereon or limiting the scope thereof.

Methods for fabricating a semiconductor device are provided and claimed. As set forth in claim 1, a method for fabricating a semiconductor device comprises forming a gate pattern and a source/drain region on a silicon substrate (See Application at page 4, lines 9-13 and 20-21, and Figs 2A at reference numerals 19, 23 and 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region

are formed (See Application at page 5, lines 1-2, and Figures 2B at reference numerals 25, 11, 19 and 23), forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide (See Application at page 5, lines 7-8 and Figures 2B at reference numerals 27, 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region (See Application at page 5, lines 20-23 and Figure. 2C at reference numerals 25, 27, 29, 19 and 23), and selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region (See Application at page 5, lines 28-31, page 6, lines 1-5 and Figure 2D at reference numerals 25, 27, 29, and 23) and whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

As set forth in claim 12, a method for fabricating a semiconductor device comprises forming a field region on a substrate to define an active region (See Application at page 4, lines 9-10 and Figure 2A at reference numerals 13 and 11), forming a gate pattern on the active region, wherein the gate pattern includes sidewalls (See Application at page 4, lines 11-15 and Figure 2A at reference numerals 19 and 13), forming spacers on the sidewalls of the gate pattern (See Application at page 4, lines 15-19 and Figure 2A at reference numerals 21 and 19), forming source/drain regions aligned with the spacers on both sides of the gate pattern (See Application at page 4, lines 20-21 and Figure 2A at reference numerals 21 and 19), cleaning the substrate using a wet cleaning process (See Application at page 4, lines 26-28 and Figure 2B at reference numeral 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate (See Application at page 5, lines 1-3 and Figure 2B at reference numerals 25, 11, 21 and 19), forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy (See Application at page 5, lines 7-8 and Figure 2B at reference numerals 27 and 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region (See Application at page 5, lines 20-24 and Figure 2C at reference numerals

11, 25 27, 29, 19 and 23), and cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 11, 25 27, 29, 19, 23 and 21), and whereby, the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, lumping of the nickel silicide is prevented, and a silicide residue is prevented from remaining on the spacers and the field region , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

Next, as set forth in claim 19, a method for fabricating a semiconductor device comprises forming a gate pattern and a source/drain region on a silicon substrate (See Application at page 4, lines 9-13, lines 20-21 and Figure 2A at reference numerals 19, 23 and 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed (See Application at page 5, lines 1-6 and Figure 2B at reference numerals 25, 11, 21, and 19), forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide (See Application at page 5, lines 7-8 and Figure 2B at reference numerals 27 and 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region (See Application at page 5, lines 20-24 and Figure 2C at reference numerals 25, 27, 29, 19 and 23), and selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 25, 27 and 29) and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-6 at reference numeral 25).

In addition, as set forth in claim 23, a method for fabricating a semiconductor device comprises forming a field region on a substrate to define an active region (See Application at page 4, lines 9-10 and Figure 2A at reference numerals 12 and 11), forming a gate pattern on the active region, wherein the gate pattern includes sidewalls (See Application at page 4, lines 11-14 and Figure 2A at reference numerals 19 and 13), forming spacers on the sidewalls of the gate pattern (See Application at page 4, lines 15-18 and Figure 2A at reference numerals 21 and 19), forming source/drain regions aligned with the spacers on both sides of the gate pattern (See Application at page 4, lines 20-21 and Figure 2A at reference numerals 21 and 19), cleaning the substrate using a wet cleaning process (See Application at page 4, lines 26-28 and Figure 2B at reference numeral 11), etching the silicon substrate using an RF sputter etching process to remove particles from the substrate (See Application on page 4, lines 29-30 and Figure 2B at reference numeral 11), forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate (See Application at page 5, lines 1-3 and Figure 2B at reference numerals 25, 11, 21 and 19), forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy (See Application at page 5, lines 7-8 and Figure 2B at reference numerals 27 and 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region (See Application at page 5, lines 20-24 and Figure 2C at reference numerals 11, 25, 27, 29, 19 and 23), and cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region exposed (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 11, 25 27, 29, 19, 23 and 21), and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

Also, as set forth in claim 31, a method for fabricating a semiconductor device comprises forming a gate pattern and a source/drain region on a silicon substrate (See Application at page 4, lines 9-13, lines 20-21 and Figure 2A at reference numerals 19, 23 and 11), forming a Ni-

based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed (See Application at page 5, lines 1-2, and Figures 2B at reference numerals 25, 11, 19 and 23), forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide (See Application at page 5, lines 7-8 and Figures 2B at reference numerals 27, 25), thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region (See Application at page 5, lines 20-23 and Figure 2C at reference numerals 25, 27, 29, 19 and 23), and selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region (See Application at page 5, lines 28-31, page 6, lines 1-3 and Figure 2D at reference numerals 25, 27, 29, and 23), and whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof (See Application at page 5, lines 1-5 at reference numeral 25).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 5-6, 12, 16-17, 27-28 and 31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,196,360 to Doan et al. ("the Doan patent") in view of U.S. Patent No. 5,766,997 to Takeuchi et al. ("the Takeuchi patent") and U.S. patent Application Publication No. 2002/0151170A1 to Maex et al. ("the Maex publication").

B. Claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Doan with Takeuchi and Maex as applied to claims 1, 5-6, 12, 16-17, 27-28 and 31 above, and further in view of U.S. Patent No. 6,503,840B2 to Catabay et al (hereinafter Catabay), U.S. Patent No. 6,664,166 B1 to Jaiswal et al (hereinafter Jaiswal) and U.S. Patent No. 6,775,046 B2 to Hill et al (hereinafter Hill).

7. ARGUMENTS

A. Claims 1, 5-6, 12, 16-17, 27-28 and 31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,196,360 to Doan et al. ("the Doan patent") in view of U.S. Patent No. 5,766,997 to Takeuchi et al. ("the Takeuchi patent") and U.S. patent Application Publication No. 2002/0151170A1 to Maex et al. ("the Maex publication").

(i) The teachings of the combination of Doan, Takeuchi and Maex fails to provide sufficient motivation, guidance or teaching to one skilled in the art to produce a method for fabricating a semiconductor device" which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in each of claims 1, 12 and 31.

Applicants maintain their position from the Appeal Brief filed on September 18, 2007 that the Doan, Takeuchi and Maex references alone or in combination fail to teach or suggest all the features recited in claims 1, 12 and 31 for at least the reasons set forth below.

As conceded by the Examiner in the Examiner's Answers to Appellants Appeal Brief dated April 13, 2009 and May 27, 2009 and the Final Office Action dated April 3, 2007, the Doan reference does not teach or suggest forming a Ni-based alloy layer comprised of a nickel alloy for silicide as recited in claims 1, 12 and 31. Further, Applicants maintain their position that the Takeuchi reference likewise fails to teach or suggest forming a nickel alloy layer for silicide.

Specifically, the Examiner has still failed to properly explain how Takeuchi teaches forming a nickel alloy layer for silicide as recited in claims 1, 12, and 31. As discussed in the Appeal Brief filed on September 18, 2007, Takeuchi's teachings are silent regarding forming an alloy anywhere in its description, let alone a nickel alloy layer for silicide, as required by claims

1, 12 and 31. Rather, Takeuchi at best only mentions that a metal layer may be formed using more than one type of metal in the same metal layer. **(See Col. 7, lines 30-37 of Takeuchi).** However, this teaching by Takeuchi is insufficient without more for teaching the use of alloys because as is well known in the art, metals may be combined to form a metal layer without that metal layer necessarily being a metal alloy layer. In other words, even when metals are mixed, alloys are not necessarily formed. Rather, additional steps are required for turning a mixture of metals into an alloy.

Furthermore, the Examiner offers additional documents such as (i) a Wikipedia definition and (ii) USPTO Classification definitions in the Advisory Action dated June 13, 2007 and the Examiner's Answer to the Appellants Appeal Brief dated April 13, 2009 in an attempt to try and support his position that Takeuchi teaches forming a nickel alloy layer for silicide. However, it respectfully submitted that these additional documents do not support the Examiner's position that Takeuchi teaches forming a nickel alloy layer for silicide as recited in claims 1, 12 and 31. Rather, the Wikipedia definition provided by the Examiner simply defines what constitutes a refractory metal but does not teach or suggest forming a nickel alloy layer for silicide from any of these refractory metals. Furthermore, the USPTO classification definition provided by the Examiner mentions certain refractory metals and that these refractory metals may be combined with one another to form alloys. However, the above-mentioned USPTO classification fails to teach or suggest forming the specific nickel based type alloy layers for silicide recited in claims 1, 12 and 31.

In sum, Takeuchi is silent regarding forming alloy layers for silicide anywhere within that reference, let alone forming the specific nickel based type alloy layers for silicide recited in claims 1, 12 and 31. Moreover, the additional documents such as the (i) Wikipedia definition and (ii) the USPTO Classification definitions provided by the Examiner fail to cure the above deficiencies of the Takeuchi reference for at least the reasons set forth above.

In addition, Applicants also maintain their position that the Maex reference fails to cure the deficiencies of the Doan and Takeuchi references for at least the reasons set forth below. As set forth in Applicants Appeal Brief dated September 18, 2007, the Maex reference's teachings are insufficient for guiding one skilled in the art to provide a Ni-based metal layer comprised of a

nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20% of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in claims 1, 12 and 31. Rather, it appears that all of the alloys discussed in Maex include at least some cobalt. In contrast, the nickel alloy layers for silicide recited in claims 1, 12 and 31 do not contain any cobalt.

In an attempt to support his position that Maex cures the deficiencies of Doan and Takeuchi mentioned above, The Examiner contends in the Examiner's Answer dated April 13, 2009 to Appellant's Appeal Brief, that Maex teaches in a passage of this reference that "...the first layer structure can also include a cobalt-nickel alloy with the nickel content varying from 0 to 100%....Also, other elements such as Pt or Pd can be chosen as elements that are present in the first layer structure...or the elements Pt and Pd can be added in minor amounts to the first layer structure. Also, other elements such as Au, Ir, Os, Rh, Ti, Ta, W, Mo, Cr, C and Ge can be part of the first layer structure. **(See Page 14 of the Examiner's Answer dated April 13, 2009).** " However, the Examiner's seems to overlook the fact that even though Maex may state that the nickel content can vary from 0 to 100%, there must still be at least some cobalt present in the alloy of the first layer structure of Maex set forth above because Maex refers to the above alloy as a cobalt-nickel alloy, and thus the Examiner's position is wholly erroneous. Consequently, since all of the alloys discussed in Maex appear to contain at least some cobalt and the nickel alloy layer for silicide recited in claims 1, 12 and 31 do not contain any cobalt, the Maex reference teaches different alloys than recited in claims 1, 12 and 31 and thus Maex cannot cure the deficiencies of the Doan and Takeuchi references.

Moreover, in addition to the reasons given above, the Maex reference's teachings are also insufficient for guiding one skilled in the art to cure the deficiencies of the Doan and Takeuchi references because Maex teaches the desirability of forming alloy layers which include nickel in amounts less than 50%, more preferably less than 15%, even less than 10% and even as low as 1%. **(See paragraphs [0014], [0019] and [0082] of Maex).** Thus, Applicants maintain their position from the Appeal Brief that one skilled in the art would likely not be motivated to form a nickel based alloy layer as required by claims 1, 12 and 31 but instead would likely only be motivated based upon the teachings of the Maex reference to form an alloy layer which was not nickel based and which included nickel in the alloy in amounts of less than 50% down to 1%.

Thus, for at least the reasons set forth above, the combination of Doan, Takeuchi and Maex at the very least fails to provide sufficient motivation, guidance or teaching to one skilled in the art to produce a method for fabricating a semiconductor device" which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in each of claims 1, 12 and 31.

Because the combination of Doan, Takeuchi and Maex fails to provide sufficient motivation, guidance or teaching to one skilled in the art to produce a method for fabricating a semiconductor device which includes each and every element recited in each of claims 1, 12 and 31, it is submitted that no *prima facie case* of obviousness has been established. Accordingly, the above rejections to claims 1, 12 and 31 under 35 U.S.C. 103(a) should be reversed for at least the above reasons. Moreover as claims 5, 6, 16, 17 and 27-28 depend from claims 1 and 12, respectively, the above rejections to these dependent claims under 35 U.S.C. 103(a) should also be reversed for at least the reasons set forth above with regard to claims 1 and 12, respectively.

B. Claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Doan with Takeuchi and Maex as applied to claims 1, 5-6, 12, 16-17, 27-28 and 31 above, and further in view of U.S. Patent No. 6,503,840B2 to Catabay et al (hereinafter Catabay), U.S. Patent No. 6,664,166 B1 to Jaiswal et al (hereinafter Jaiswal) and U.S. Patent No. 6,775,046 B2 to Hill et al (hereinafter Hill).

(i) The teachings of the combination of Doan, Takeuchi, and Maex with Catabay, Jaiswal and/or Hill fails to provide sufficient motivation, guidance or teaching to one skilled in the art to produce a method for fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof as essentially recited in each of claims 2, 7-8, 13, 18-19, 22- 23, 26 and 29-30.

As set forth above in connection with claims 1, 12 and 31, the combination of Doan, Takeuchi and Maex fails to provide sufficient motivation, guidance or teaching to one skilled in the art to utilize a method of fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof. Thus, the combination of Doan, Takeuchi and Maex likewise at the very least also fails to provide sufficient motivation, guidance or teaching to one skilled in the art to utilize a method of fabricating a semiconductor device which includes forming a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination there, as essentially recited in each of claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30 for essentially the same reasons as set forth above with regard to claims 1, 12 and 31. **(See discussion above with regard to claims 1, 12 and 31).**

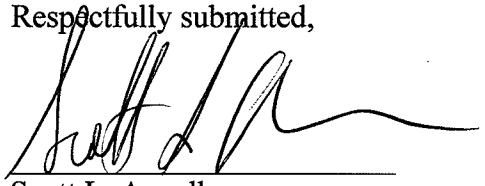
Lastly, Applicants also maintain that Catabay, Jaiswal and Hill references each fail to cure the above noted deficiencies of the Doan, Takeuchi and Maex references because at the very least Catabay, Jaiswal and Hill are each silent regarding a method of fabricating a semiconductor device, which includes a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof , as essentially recited in each of claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30. Therefore, a combination of Doan Takeuchi and Maex with Catabay, Jaiswal and/or Hill fails to provide sufficient motivation, guidance or teaching to one skilled in the art to produce a method of fabricating a semiconductor device, which includes a Ni-based metal layer comprised of the nickel alloy for silicide which is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof , as essentially recited in each of claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30.

Because the combination of Doan, Takeuchi and Maex with Catabay, Jaiswal and/or Hill fails to provide sufficient motivation, guidance or teaching to one skilled in the art to produce a method for fabricating a semiconductor device which includes each and every element recited in each of claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30, it is submitted that no *prima facie case* of obviousness has been made. Accordingly, the above rejections to claims 2, 7-8, 13, 18-19, 22-23, 26 and 29-30 under 35 U.S.C. 103(a) should be reversed for at least the above reasons.

Conclusion

The references of Doan, Takeuchi, Maex, Catabay, Jaiswal and/or Hill cited by the Examiner, taken individually or in combination fail to teach or suggest all of the features recited in independent claims 1, 12, 19, 23 and 31. Claims 2 , 5-8 and 27 depend from claim 1, claims 13 , 16-18 and 28 depend from claim 12, claims 22 and 29 depend from claim 19 and claims 26 and 30 depend from claim 23. The dependent claims are believed to be allowable for at least the reasons given for independent claims 1, 12, 19 and 23. Accordingly, it is respectfully requested that the Board reverse all rejections of claims 1, 2, 5-8, 12-13, 16-19, 22-23 and 26-31 under 35 U.S.C. 103(a).

Respectfully submitted,



Scott L. Appelbaum
Reg. No. 41,587
Attorney for Applicants

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797
Tel: (516) 692-8888
Fax: (516) 692-8889

CLAIMS APPENDIX

1. (previously presented) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region,

whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

2. (original) The method as claimed in claim 1, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

3. (canceled)

4. (canceled)

5. (original) The method as claimed in claim 1, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

6. (original) The method as claimed in claim 1, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

7. (original) The method as claimed in claim 1, further comprises etching the silicon substrate using an RF sputter stching process to remove particles from the substrate after forming the source/drain.

8. (original) The method as claimed in claim 7, wherein the RF sputter etching process comprises forming the Ni-based metal layer for silicide and the N-rich titanium nitride layer in-situ.

Claims 9-11 (Canceled)

12. (Previously presented) A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region,

whereby, the nickel silicide on the gate pattern is neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region,

lumping of the nickel silicide is prevented, and a silicide residue is prevented from remaining on the spacers and the field region , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

13. (original) The method as claimed in claim 12, wherein the Ni-based metal layer for silicide is formed at a temperature of about 25 °C to about 500 °C.

14. (canceled)

15. (Canceled)

16. (original) The method as claimed in claim 12, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

17. (original) The method as claimed in claim 12, wherein the thermal treatment for forming the nickel silicide layer is carried out using a rapid thermal treatment system, a furnace, a sputter system, or any combination thereof.

18. (original) The method as claimed in claim 12, further comprises etching the silicon substrate using an RF sputter etching process to remove particles from the substrate after forming the source/drain region.

19. (previously presented) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide at a temperature of about 25 °C to about 500 °C on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

20. (canceled)

21. (Canceled)

22. (Previously presented) The method as claimed in claim 19, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

23. (previously presented) A method for fabricating a semiconductor device comprising:

forming a field region on a substrate to define an active region;

forming a gate pattern on the active region, wherein the gate pattern includes sidewalls;

forming spacers on the sidewalls of the gate pattern;

forming source/drain regions aligned with the spacers on both sides of the gate pattern;

cleaning the substrate using a wet cleaning process;

etching the silicon substrate using an RF sputter etching process to remove particles from the substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region; and

cleaning the substrate to selectively to remove the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer and to expose a top portion of the nickel silicide layer formed on the gate pattern and the source/drain region exposed , and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Ti, Hf, W, Pt, Pd, V, Nb, or any combination thereof.

24. (canceled)

25. (canceled)

26. (previously presented) The method as claimed in claim 23, wherein the N/Ti ratio of the N-rich titanium nitride layer ranges from about 0.5 to about 2.

27. (previously presented) The method of claim 1, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

28. (previously presented) The method of claim 12, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

29. (previously presented) The method of claim 19, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

30. (previously presented) The method of claim 23, wherein the nickel alloy layer includes greater than 0 to about 20 % of only one of the materials of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

31. (previously presented) A method for fabricating a semiconductor device comprising:

forming a gate pattern and a source/drain region on a silicon substrate;

forming a Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate where the gate pattern and the source/drain region are formed;

forming an N-rich titanium nitride layer on the Ni-based metal layer comprised of the nickel alloy for silicide;

thermally treating the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to form a nickel silicide layer on each of the gate pattern and the source/drain region; and

selectively removing the Ni-based metal layer comprised of the nickel alloy for silicide and the N-rich titanium nitride layer to expose a top portion of the nickel silicide on the gate pattern and the source/drain region,

whereby the nickel silicide on the gate pattern is neither shorted nor cut, and lumping of the nickel silicide is prevented, and wherein the Ni-based metal layer comprised of the nickel alloy for silicide is a nickel alloy layer including greater than 0 to about 20 % of a material selected from the group consisting essentially of Ta, Zr, Hf, Pt, Pd, V, Nb, or any combination thereof.

EVIDENCE APPENDIX:

None

RELATED PROCEEDINGS APPENDIX :

None